

WHAT IS CLAIMED IS:

1 1. For use in a base station (BS) of a fixed wireless
2 network capable of communicating with a plurality of subscriber
3 transceivers via time division duplex (TDD) channels, a BS
4 transceiver comprising:

5 a receiver front-end capable of receiving data burst
6 transmissions from said plurality of subscriber transceivers in an
7 uplink portion of a TDD channel, wherein said receiver front-end
8 demodulates said received data burst transmissions into a digital
9 baseband signal in-phase (I) signal and a digital baseband
10 quadrature (Q) signal;

11 a first frequency domain feedforward equalization filter
12 capable of receiving said I signal and performing a Fast Fourier
13 Transform on a block of N symbols in said I signal to produce a
14 first symbol estimate sequence;

15 a second frequency domain feedforward equalization filter
16 capable of receiving said Q signal and performing a Fast Fourier
17 Transform on a block of N symbols in said Q signal to produce a
18 second symbol estimate sequence;

19 an adder capable of receiving said first signal estimate
20 sequence on a first input and said second signal estimate sequence
21 on a second input and producing a combined symbol estimate
22 sequence;

23 a slicer capable of receiving and quantizing said
24 combined symbol estimate sequence to produce a sequence of decided
25 symbols; and

26 a time domain feedback filter capable of receiving said
27 sequence of decided symbols and generating a symbol correction
28 sequence that is applied to a third input of said adder.

1 2. The BS transceiver as set forth in Claim 1 wherein said
2 first frequency domain feedforward equalization filter is $2/T$
3 fractionally spaced, where T is a period of said block of said N
4 symbols.

1 3. The BS transceiver as set forth in Claim 2 wherein said
2 second frequency domain feedforward equalization filter is $2/T$
3 fractionally spaced, where T is a period of said block of said N
4 symbols.

1 4. The BS transceiver as set forth in Claim 1 wherein said
2 time domain feedback filter comprises a delay line comprising D
3 delay taps.

1 5. The BS transceiver as set forth in Claim 4 wherein said
2 time domain feedback filter uses C feedback coefficients to
3 generate said symbol correction sequence, where C is less than D.

1 6. The BS transceiver as set forth in Claim 5 wherein said
2 feedback filter is a RAKE filter.

1 7. The BS transceiver as set forth in Claim 1 further
2 comprising a channel estimation circuit capable of detecting a
3 preamble sequence of symbols in at least one of said I and Q
4 signals and producing therefrom a first plurality of feedforward
5 coefficients usable by said first frequency domain feedforward
6 equalization filter.

1 8. The receiver as set forth in Claim 7 wherein said channel
2 estimation circuit produces a second plurality of feedforward
3 coefficients usable by said first frequency domain feedforward
4 equalization filter.

1 9. The receiver as set forth in Claim 1 wherein N=16.

1 10. A fixed wireless network comprising:

2 a plurality of base stations capable of communicating
3 with a plurality of subscriber transceivers via time division
4 duplex (TDD) channels, each said base station having a base station
5 (BS) transceiver comprising:

6 a receiver front-end capable of receiving data burst
7 transmissions from said plurality of subscriber transceivers
8 in an uplink portion of a TDD channel, wherein said receiver
9 front-end demodulates said received data burst transmissions
10 into a digital baseband signal in-phase (I) signal and a
11 digital baseband quadrature (Q) signal;

12 a first frequency domain feedforward equalization
13 filter capable of receiving said I signal and performing a
14 Fast Fourier Transform on a block of N symbols in said I
15 signal to produce a first symbol estimate sequence;

16 a second frequency domain feedforward equalization
17 filter capable of receiving said Q signal and performing a
18 Fast Fourier Transform on a block of N symbols in said Q
19 signal to produce a second symbol estimate sequence;

20 an adder capable of receiving said first signal
21 estimate sequence on a first input and said second signal
22 estimate sequence on a second input and producing a combined
23 symbol estimate sequence;

24 a slicer capable of receiving and quantizing said
25 combined symbol estimate sequence to produce a sequence of
26 decided symbols; and

27 a time domain feedback filter capable of receiving
28 said sequence of decided symbols and generating a symbol
29 correction sequence that is applied to a third input of said
30 adder.

1 11. The fixed wireless network as set forth in Claim 10
2 wherein said first frequency domain feedforward equalization filter
3 is $2/T$ fractionally spaced, where T is a period of said block of
4 said N symbols.

1 12. The fixed wireless network as set forth in Claim 11
2 wherein said second frequency domain feedforward equalization
3 filter is $2/T$ fractionally spaced, where T is a period of said
4 block of said N symbols.

1 13. The fixed wireless network as set forth in Claim 10
2 wherein said time domain feedback filter comprises a delay line
3 comprising D delay taps.

1 14. The fixed wireless network as set forth in Claim 13
2 wherein said time domain feedback filter uses C feedback
3 coefficients to generate said symbol correction sequence, where C
4 is less than D.

1 15. The fixed wireless network as set forth in Claim 14
2 wherein said feedback filter is a RAKE filter.

1 16. The fixed wireless network as set forth in Claim 10
2 further comprising a channel estimation circuit capable of
3 detecting a preamble sequence of symbols in at least one of said I
4 and Q signals and producing therefrom a first plurality of
5 feedforward coefficients usable by said first frequency domain
6 feedforward equalization filter.

1 17. The fixed wireless network as set forth in Claim 16
2 wherein said channel estimation circuit produces a second plurality
3 of feedforward coefficients usable by said first frequency domain
4 feedforward equalization filter.

1 18. The fixed wireless network as set forth in Claim 10
2 wherein $N=16$.

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